Republic of Iraq
The Ministry of Higher Education & Scientific Research
2024-2023

Flow up of implementation Syllabus for Logic Design

University: Thi-Qar
College: Pure Science
Department: Computer Science
Stage: First
Lecturer name: Kadhim Abbas
Academic Status: Lecturer
Qualification: Ph.D. in Mech. Engg.
Place of work: Thi-Qar University

Course Instructor	Dr. Kadhim Abbas Jabbar				
E_mail	Kadhimabass.comp@utq.edu.iq				
Title	Logic Design				
Course Coordinator	Dr. Wissam Abbas				
Course Objective	1-Able to perform the conversion among different number systems; Familiar with baisc logic gates -- AND, OR & NOT, XOR, XNOR; Independently or work in team to build simple logic circuits using basic. 2-Able to design simple combinational logics using baisc gates. 3-Able to optimize simple logic using Karnaugh maps, understand "don't care". 4-Familiar with basic combinational and sequential components used in the typical datapath designs: Register, Adders, Shifters, Comparators; Counters, Multiplier, Arithmetic-Logic Units (ALUs), RAM. Able to do simple register-transfer level (RTL) design.				
Course Description	Number systems, arithmetic operations, decimal codes, alphanumeric codes, Boolean algebra, Karnaugh maps, NAND and NOR gates, exclusive-OR gates, integrated circuits, combinational circuits, decoders, encoders, multiplexers, adders, subtractors, multipliers, sequential circuits, latches, flip-flops, sequential circuits analysis, registers, counters, RAM and ROM memories, programmable logic technologies.				
Textbook	1- Digital Logic Fundamentals 9th edition (Thomas L. Floyd) 2- Digital Logic And Computer Design By M. Morris Mano				
Course Assessment	Term Tests	Laboratory	Quizzes	Project	Final Exam
	30%	15%	5%	-	50%
General Notes					

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Course weekly Outline

week	Date		Lab. Experiment Assignments	Notes
1	17/9/2023	Decimal &Binary Numbers		
2	24/9/2023	Octal & Hexadecimal Numbers		
3	01/10/2023	Decimal to Binary, Octal & Hexadecimal Conversions		
4	08/10/2023	Addition, Subtraction of Numbers		
5	15/10/2023	Using 1's &2's Complements in subtraction		
6	22/10/2023	Multiplication & Divisions of Binary Numbers		
7	29/10/2023	BCD, Excess3 & Gray Coding Systems		
8	05/11/2023	Code, Parity & Seven Segments		
9	12/11/2023	Logic Gates & Truth Table		
10	19/11/2023	Boolean Operations & Expressions		
11	26/11/2023	Boolean Analysis of Logic Circuits		
12	03/12/2023	Simplification of Logic Circuits Using Boolean Rules		
13	10/12/2023	DeMorgan's Theorem &Simplifications of Logic Circuits using DeMorgan's		
14	17/12/2023	Karnaugh Map		
15	24/1/2023	Exams		
16	31/1/2023	Exams		

Half-year Break

17	28/1/2024	Karnaugh Map SOP & POS Minimizations		
18	04/2/2024	Design of a Simple digital System Using Karnaugh Map		
19	11/2/2024	Addition Operation Using Full & Half Adder		
20	18/2/2024	Half & Full Subtractor		
21	25/2/2024	Multiplexer & Demultiplexer		
22	03/3/2024	Flip-Flops Operating Characteristics		
23	10/3/2024	Flip-Flop Applications		
24	17/3/2024	Shift Register Functions & Their Types		
25	24/3/2024	Shift Registers in Logic Circuits		
26	31/3/2024	Counter Operation		
27	07/4/2024	Types of Counters		
28	14/4/2024	Counter Applications		
29	21/4/2024	RAMs & Their Types		
30	28/4/2024	ROMs & Their Types		
31	05/5/2024	Comparison between ROMs & RAMs		
32	12/5/2024	Exams		

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تؤيد اللجنة العلمية مطابقة الخطة التدريسية لمفردات منهج المادة الدراسية

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Instructor Signature(Lab.) **Instructor Signature(Theoretical)**

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1st Scientific committee member **2nd Scientific committee member** **3rd Scientific committee member**

....

Head of Scientific committee **Dean**

ملاحظة: أعدت الاستمارة أستنادا الى كتاب وزارة التعليم العالي والبحث العلمي، جهاز الاشراف والتقويم العلمي، دائرة ضمان الجودة والاعتماد الاكاديمي، قسم تقويم الاداء ..... ج د ت / 1860 في تاريخ 02/ 10/ 2014