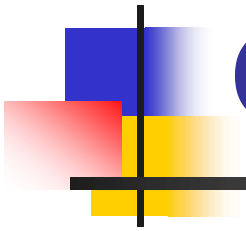
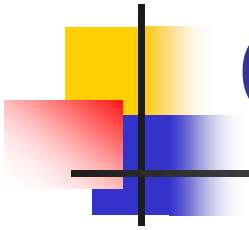


Unit 6 Part I
CPU Organization



Central Processing Unit

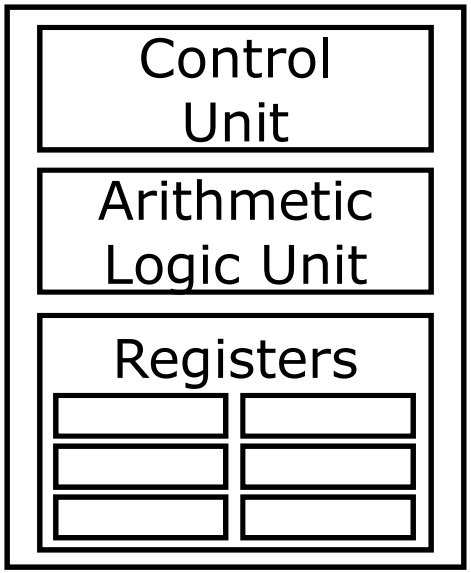
- The part of the computer performs the bulk of data processing operations is called the central processing unit

- The CPU is made up of three major parts:
  - Register set
  - ALU
  - Control units

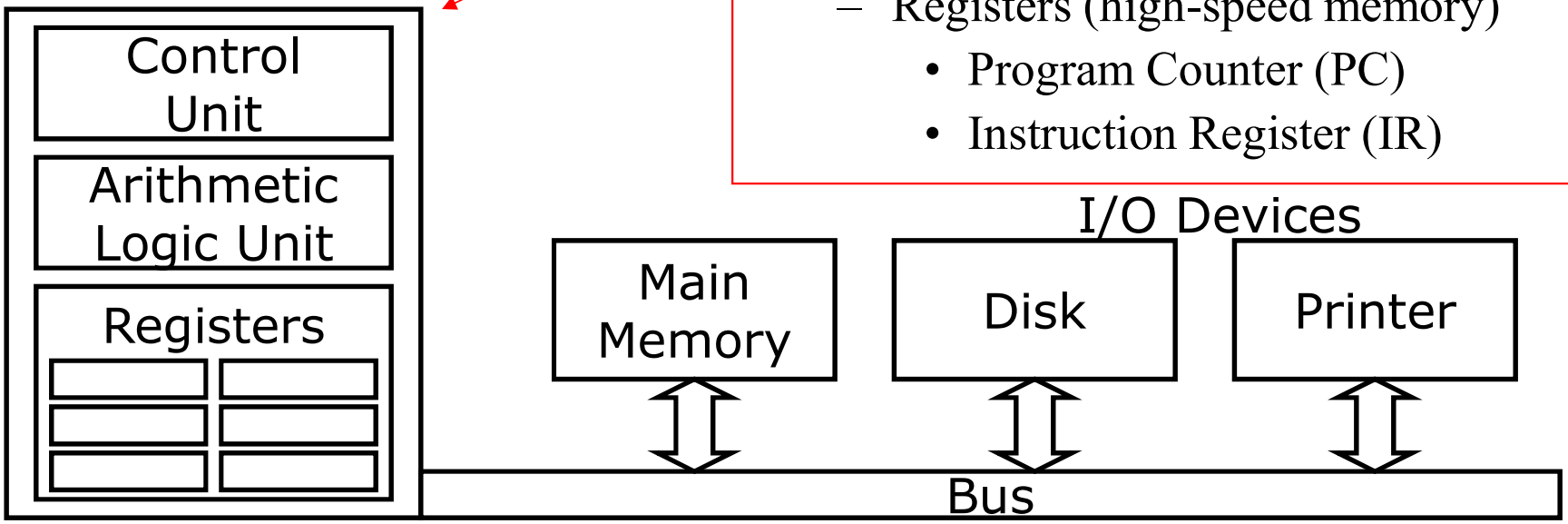
CPU

The **central processing unit (CPU)** of a computer is the main unit that dictates the rest of the computer organization

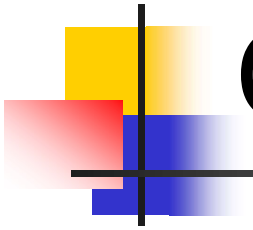
- 1. **Register se**t: Stores intermediate data during the execution of instructions;
- 2. **Arithmetic logic unit (ALU**): Performs the required micro-operations for executing the instructions;
- 3. **Control uni**t: supervises the transfer of information among the registers and instructs the ALU as to which operation to perform by generating control signals.



- Central Processing Unit = “brain”
- Executes programs by:
  - Fetching and decoding the next instruction from memory
  - Execute it
- Consists of:
  - Control Unit
  - Arithmetic Logic Unit (ALU)
  - Registers (high-speed memory)
    - Program Counter (PC)
    - Instruction Register (IR)



8-2. General Register Organization

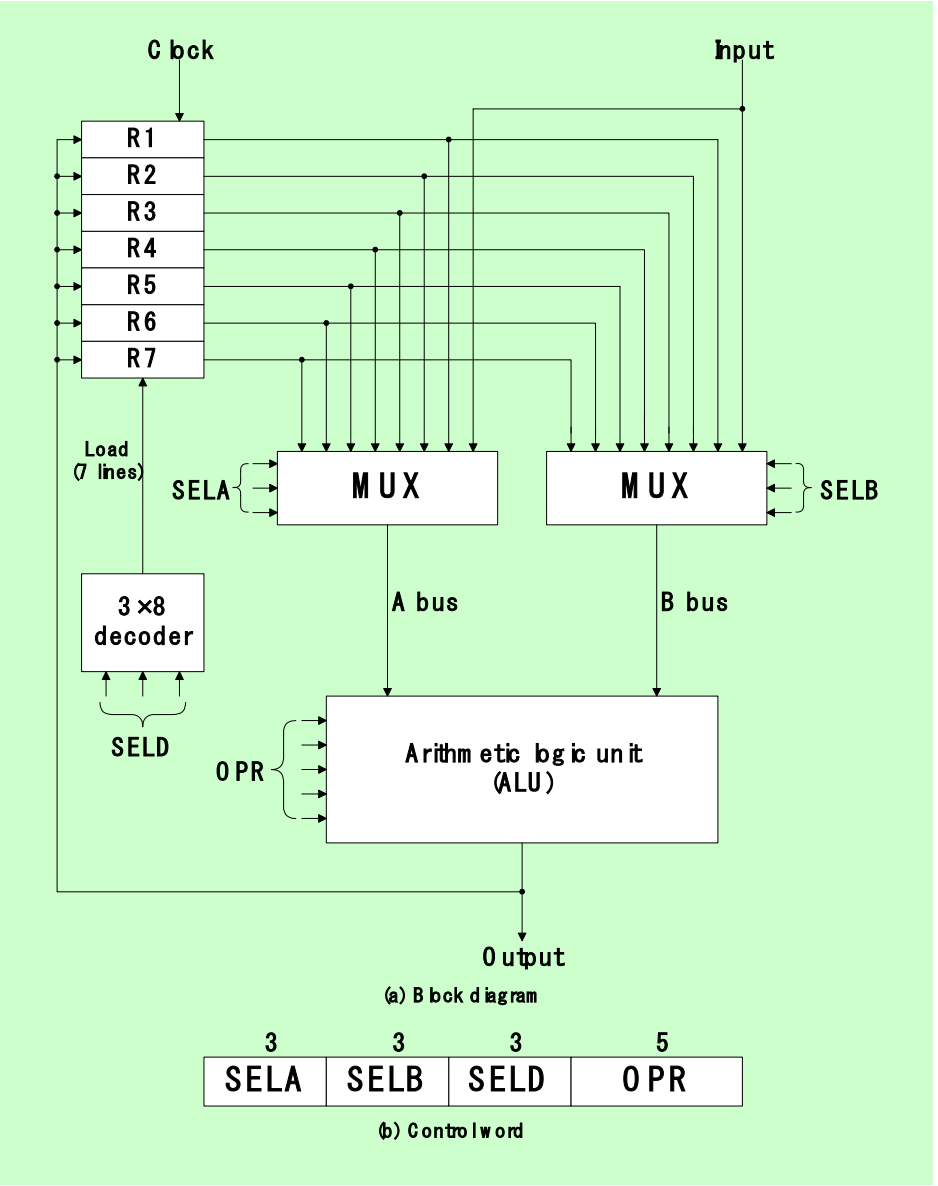


- CPU must have some working space (fast access and close to CPU)
- This space is efficiently used to store intermediate values
- The most convenient way to communicate registers is trough common bus system

8-2. General Register Organization

Bus organization for 7 CPU registers:

- 2 MUX
- BUS A and BUS B
- ALU
- 3 X 8 Decoder

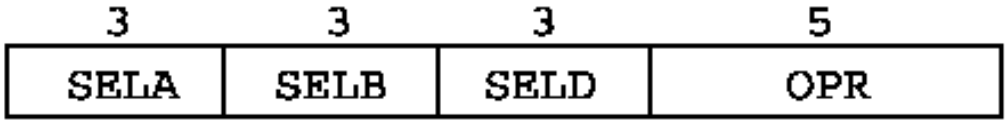


8-2. General Register Organization

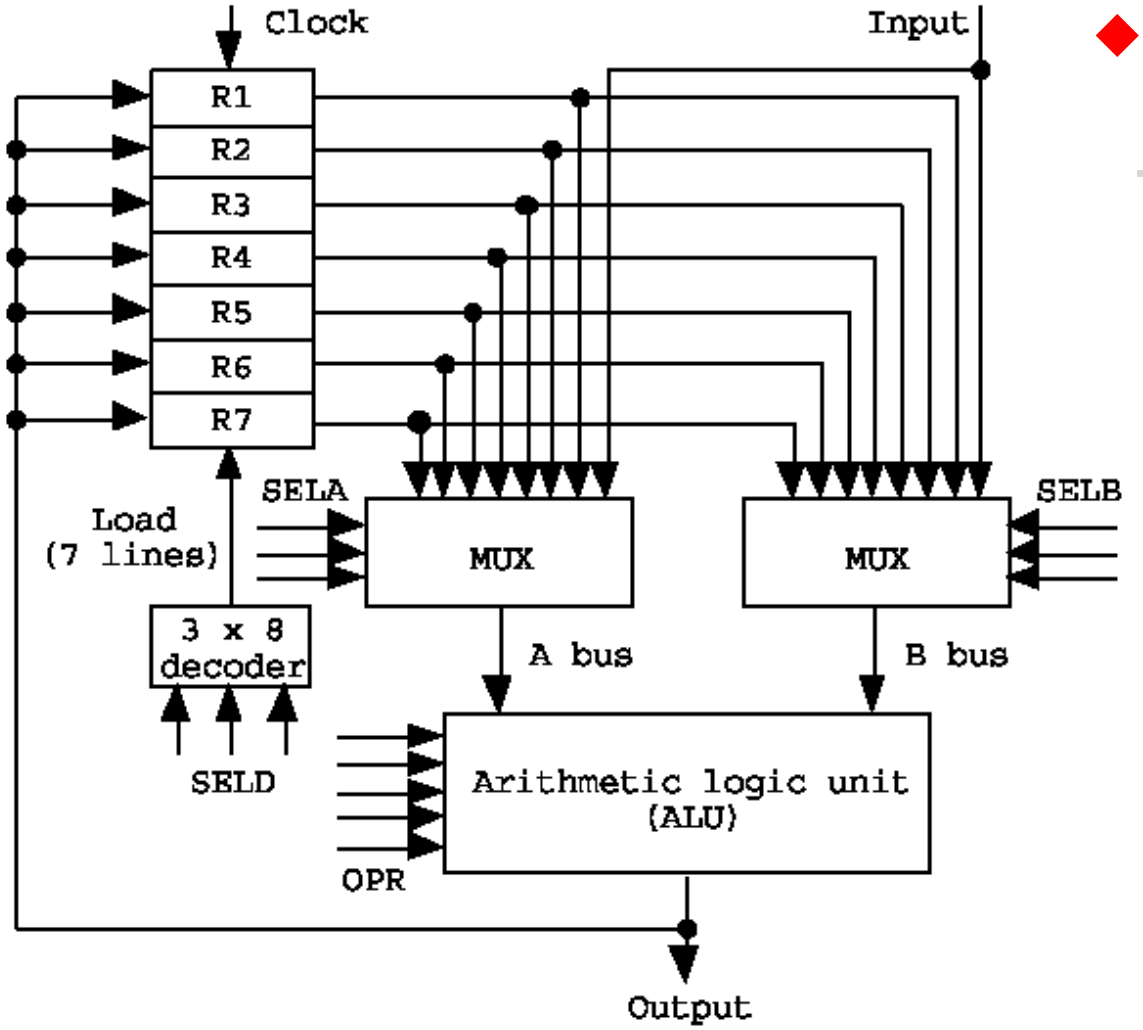
- Bus organization for 7 CPU registers:
  - **2 MUX**: select one of 7 register or external data input by **SELA** and **SELB**
  - **BUS A and BUS B** : form the inputs to a common ALU
  - **ALU** : **OPR** determine the arithmetic or logic microoperation
    - The result of the microoperation is available for external data output and also goes into the inputs of all registers
  - **3 X 8 Decoder**: select the register (by **SELD**) that receives the information from ALU

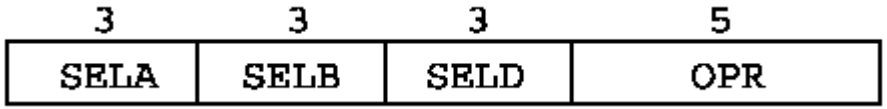
8-2. General Register Organization

- An operation is selected by the ALU **operation selector** (OPR).
- The result of a microoperation is directed to a destination register selected by a **decoder** (SELD).
- **Control word**: The 14 binary selection inputs (3 bits for SELA, 3 for SELB, 3 for SELD, and 5 for OPR)



Example 1





$R1 \leftarrow R2 + R3$

- Binary selector input
  - 1) MUX A selector (**SELA**) : to place the content of R2 into BUS A
  - 2) MUX B selector (**SELB**) : to place the content of R3 into BUS B
  - 3) ALU operation selector (**OPR**) : to provide the arithmetic addition R2 + R3
  - 4) Decoder selector (**SELD**) : to transfer the content of the output bus into R1

- Encoding of the register selection fields

Binary code	SELA	SELB	SELD
000	External input	External input	External input
001	R1	R1	R1
010	R2	R2	R2
011	R3	R3	R3
100	R4	R4	R4
101	R5	R5	R5
110	R6	R6	R6
111	R7	R7	R7

- Encoding of the ALU operation field

OPR select	Operation	Symbol
00000	Transfer A	TSFA
00001	Increment A	INCA
00010	Add A + B	ADD
00101	Subtract A - B	SUB
00110	Decrement A	DECA
01000	AND A and B	AND
01010	OR A and B	OR
01100	XOR A and B	XOR
01110	Complement A	COMA
10000	Shift right A	SHRA
11000	Shift left A	SHLA

- Encoding of Register Selection Fields:
  - »**SELA** or **SELB** = 000 (External **Input**) : MUX selects the external data
  - »**SELD** = 000 (**None**) : no destination register is selected but the contents of the output bus are available in the external output

Example

(Example 2)

1. Micro-operation

R1 ← R2 - R3

2. Control word

Field:	SELA	SELB	SELD	OPR
Symbol:	R2	R3	R1	SUB
Control word:	010	011	001	00101